EXPERIMENT NO. 3: SINGLE-STAGE BJT AMPLIFIER CHARACTERIZATION

1.0 AIM:

The primary aim of this experiment is to meticulously design, construct, and comprehensively characterize the performance of a common-emitter (CE) Bipolar Junction Transistor (BJT) amplifier. This characterization will encompass its fundamental DC biasing, mid-band AC parameters (voltage gain, input impedance, output impedance), and its frequency response across the entire operational spectrum, allowing for the determination of its bandwidth.

2.0 OBJECTIVES:

Upon successful completion of this experiment, you will be able to:

- **Design Proficiency: Design a stable voltage divider bias circuit for a BJT common-emitter amplifier to establish a precise and stable DC operating point (Q-point).**
- **Theoretical Calculation: Accurately calculate the theoretical mid-band voltage gain (A_v), input resistance (R_{in}), and output resistance (R_{out}) of the CE amplifier utilizing the small-signal equivalent circuit (r-e model).**
- **Circuit Implementation: Construct the designed common-emitter amplifier on a breadboard following standard practices.**
- **Mid-Band Analysis: Apply a small AC signal at a designated mid-band frequency, and then experimentally measure the input and output voltages using an oscilloscope to determine the amplifier's mid-band voltage gain.**
- **Impedance Measurement: Employ appropriate experimental techniques (e.g., source resistance variation for R_{in}, load resistance variation for R_{out}) to measure the amplifier's input and output resistances.**
- **Frequency Response Analysis: Systematically vary the input signal frequency from very low to very high ranges, measuring the corresponding output voltage at each frequency point, to gather data for a frequency response plot.**
- **Bode Plot Generation: Plot the amplifier's gain (in decibels) versus frequency on a semi-log graph paper, creating a Bode plot.**
- **Bandwidth Determination: From the generated frequency response plot, accurately determine the lower cutoff frequency (f_L), the upper cutoff frequency (f_H), and subsequently calculate the amplifier's bandwidth ($BW=f_H-f_L$).**
- **Capacitor Impact: Qualitatively observe and explain the significant impact of coupling capacitors (C_C) and bypass capacitors (C_E) on the amplifier's overall frequency response characteristics.**

- **Instrumentation Skills: Gain practical experience in effectively utilizing essential laboratory equipment such as the DC power supply, AC function generator, Digital Multimeter (DMM), and Oscilloscope for detailed circuit characterization.**

3.0 APPARATUS REQUIRED:

A comprehensive list of components and equipment necessary for performing this experiment.

S. No.	Component/Equipment	Specifications/Value	Quantity
1.	DC Power Supply (Variable)	0-30V, Dual Output (for V_CC and potential V_BB)	1
2.	AC Function Generator	Sine wave, Adjustable Amplitude (0-20Vp-p), Wide Frequency Range (10Hz-1MHz)	1
3.	Digital Multimeter (DMM)	Multi-function (Voltage, Current, Resistance)	1
4.	Oscilloscope	Dual Trace, Minimum 20MHz Bandwidth	1
5.	Breadboard	Standard Size, for circuit prototyping	1
6.	NPN Bipolar Junction Transistor	BC547 (Commonly available, high gain) or equivalent	1
7.	Resistors (Carbon Film, 1/4W)	Standard E24 Series: 100 Ω, 1 kΩ, 2.2 kΩ, 4.7 kΩ, 10 kΩ, 47 kΩ, 56 kΩ, 68 kΩ (as per design needs)	Assorted
8.	Capacitors (Electrolytic)	Coupling Capacitors: 1 µF, 10 µF (25V or 50V rating)	2 (at least)
9.	Capacitors (Electrolytic)	Bypass Capacitor: 100 µF, 470 µF (25V or 50V rating)	1
10.	Potentiometer (Optional)	10 kΩ (For easy variation during R_in, R_out measurements)	1
11.	Connecting Wires	Breadboard jumper wires, various lengths	Assorted

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4.0 THEORY AND FUNDAMENTALS:

This section delves into the detailed theoretical underpinnings of the common-emitter BJT amplifier, providing all necessary formulas and explanations for a thorough understanding.

4.1 The Bipolar Junction Transistor (BJT) as an Amplifier: Fundamentals

A BJT is a three-terminal (Emitter, Base, Collector) semiconductor device capable of current amplification. A small current or voltage applied to the base terminal can control a much larger current flowing between the collector and emitter, making it suitable for amplification.

- **Transistor Types: BJTs come in NPN and PNP configurations. For an NPN transistor (like the BC547), the base is p-type, and the emitter and collector are n-type. Current flows from collector to emitter (I_C) when a positive voltage is applied to the collector relative to the emitter, and a small positive voltage is applied to the base relative to the emitter (V_BE).**
- **Operating Regions: To function as a linear amplifier, the BJT must operate in the active region. This implies:**
  - **The Base-Emitter (BE) junction must be forward biased (V_BEapprox0.7V for silicon transistors at room temperature). This allows current to flow from base to emitter (I_B).**
  - **The Base-Collector (BC) junction must be reverse biased ($V\_{BC} \< 0V$). This ensures that the collector acts as a current sink.**
- **Current Relationships: In the active region, the collector current (I_C) is directly proportional to the base current (I_B) by the DC current gain beta_DC (also called h_FE): I_C=beta_DCI_B The emitter current (I_E) is the sum of base and collector currents: I_E=I_B+I_C=I_B+beta_DCI_B=(1+beta_DC)I_B Alternatively, I_CapproxI_E if beta_DC is large (typically beta_DC50).**

4.2 DC Biasing: Establishing the Operating Point (Q-point)

Proper DC biasing is crucial to set the transistor's quiescent (no-signal) operating point, or Q-point, which is defined by the DC collector current (I_C) and collector-emitter voltage (V_CE). The Q-point must be stable and centrally located on the DC load line to allow maximum undistorted AC signal swing without entering saturation or cutoff regions.

4.2.1 Voltage Divider Bias (Most Stable Biasing Method)

This biasing technique provides excellent stability against variations in transistor parameters (like beta) and temperature.

- **Circuit Components: It uses two resistors (R_1 and R_2) to form a voltage divider at the base, and an emitter resistor (R_E) for negative feedback. A collector resistor (R_C) limits the collector current and develops the output voltage.**

- **DC Analysis Steps (Example Calculation): Let's assume a supply voltage V_CC (e.g., +12V) and we want to set I_Capprox2textmA. A typical NPN BJT (like BC547) might have beta_DC around 100 to 200. Let's use beta_DC=150 for design.**
    - **Set Emitter Voltage (V_E): For good stability, V_E is usually set to about 10% to 20% of V_CC. Let's target V_Eapprox1.2V for V_CC=12V.**
    - **Calculate Emitter Resistor (R_E): I_EapproxI_C=2textmA R_E=fracV_EI_E=frac1.2V2textmA=600Omega. *Choose the nearest standard resistor value, e.g., R_E=560Omega or 680Omega. Let's choose R_E=560Omega. Now, V_E=I_ER_Eapprox(2textmA)times(560Omega)=1.12V.***
    - **Calculate Base Voltage (V_B): V_B=V_E+V_BE (where V_BEapprox0.7V for silicon NPN) V_B=1.12V+0.7V=1.82V.**
    - **Calculate Base Divider Resistors (R_1, R_2): To ensure the voltage divider is stiff (not significantly loaded by the base current), the current through R_1 and R_2 should be much larger than I_B. A common rule is that the current through R_2 (I_R2) should be at least 10timesI_B. I_B=I_C/beta_DC=2textmA/150approx0.0133textmA. So, I_R2approx10times0.0133textmA=0.133textmA. Now, R_2=fracV_BI_R2=frac1.82V0.133textmAapprox13.68kOmega. *Choose a standard value for R_2, e.g., R_2=10kOmega or 15kOmega. Let's choose R_2=10kOmega.* Then, I_R2=frac1.82V10kOmega=0.182textmA. This is still ggI_B. Now, calculate R_1: The current through R_1 is I_R1=I_R2+I_B=0.182textmA+0.0133textmA=0.1953textmA. R_1=fracV_CC−V_BI_R1=frac12V−1.82V0.1953textmA=frac10.18V0.1953textmAapprox52.12kOmega. *Choose a standard value for R_1, e.g., R_1=56kOmega. Recalculate V_B with chosen R_1,R_2: V_B=V_CCfracR_2R_1+R_2=12Vfrac10kOmega56kOmega+10kOmega=12Vfrac1066approx1.818V. This is very close to our target 1.82V.***
    - **Calculate Collector Resistor (R_C): For maximum symmetrical output swing, V_CE is typically set to roughly half of the available voltage swing, which is V_CC−V_E. So, V_CEapproxfracV_CC−V_E2. V_CE=frac12V−1.12V2=frac10.88V2=5.44V. The voltage drop across R_C is V_RC=V_CC−V_C. We also know V_C=V_CE+V_E. So, V_RC=V_CC−(V_CE+V_E)=12V−(5.44V+1.12V)=12V−6.56V=5.44V. R_C=fracV_RCI_C=frac5.44V2textmA=2.72kOmega. *Choose a nearest standard resistor value, e.g., R_C=2.7kOmega or 2.2kOmega. Let's pick R_C=2.7kOmega.***
    - **Final Q-point Check (with chosen standard values): Using R_1=56kOmega, R_2=10kOmega, R_E=560Omega, R_C=2.7kOmega, V_CC=12V, V_BE=0.7V, beta=150: V_B=12timesfrac10k56k+10kapprox1.818V V_E=V_B−0.7Vapprox1.118V I_CapproxI_E=fracV_ER_E=frac1.118V560Omegaapprox1.996textmA V_C=V_CC−I_CR_C=12V−(1.996textmAtimes2.7kOmega)approx12V−5.389V=6.611V V_CE=V_C−V_E=6.611V−1.118V=5.493V This Q-point (I_Capprox2textmA, V_CEapprox5.5V) is well within the active region and suitable for amplification.**

4.3 AC Small-Signal Analysis: Characterizing Amplifier Gain and Impedances

For analyzing the amplifier's response to small AC signals, we replace the BJT with its small-signal equivalent model (r-e model is commonly used). DC voltage sources are considered AC grounds, and capacitors are treated as AC shorts at mid-band frequencies.

- **AC Emitter Resistance (r_e′): This represents the dynamic resistance of the forward-biased base-emitter junction. It's crucial for gain calculations. r_e′=fracV_TI_E Where V_T is the thermal voltage (V_Tapprox26textmV at room temperature, 300K), and I_E is the quiescent (DC) emitter current.**
- **AC Voltage Gain (A_v): For a common-emitter amplifier with an emitter bypass capacitor (C_E effectively shorts R_E for AC), the mid-band voltage gain is: A_v=fracv_outv_in=−fracR_C∣∣R_Lr_e′ Where:**
  - **R_C: Collector resistor.**
  - **R_L: External AC load resistance connected at the output. If no external load is connected, R_L=infty, so R_C∣∣infty=R_C.**
  - **The negative sign indicates a 180-degree phase shift between the input and output voltage signals.**
- **Input Resistance (R_in): This is the equivalent resistance seen by the AC signal source looking into the amplifier's input terminals. R_in=R_B∣∣(beta_acr_e′) Where:**
  - **R_B=R_1∣∣R_2=fracR_1timesR_2R_1+R_2 (the parallel combination of the base biasing resistors).**
  - **beta_ac: The AC current gain of the transistor (also often denoted as h_fe). For most practical purposes, beta_acapproxbeta_DC.**
- **Output Resistance (R_out): This is the equivalent resistance seen by the load looking back into the amplifier's output terminals. R_out=R_C (assuming the transistor's intrinsic output resistance, r_o, is much larger than R_C, which is a common approximation for CE amplifiers).**

4.4 Frequency Response of the CE Amplifier: Bandwidth and Cutoff Frequencies

An amplifier does not amplify all frequencies equally. Its gain typically remains constant over a range of frequencies (the mid-band) and then decreases at very low and very high frequencies.

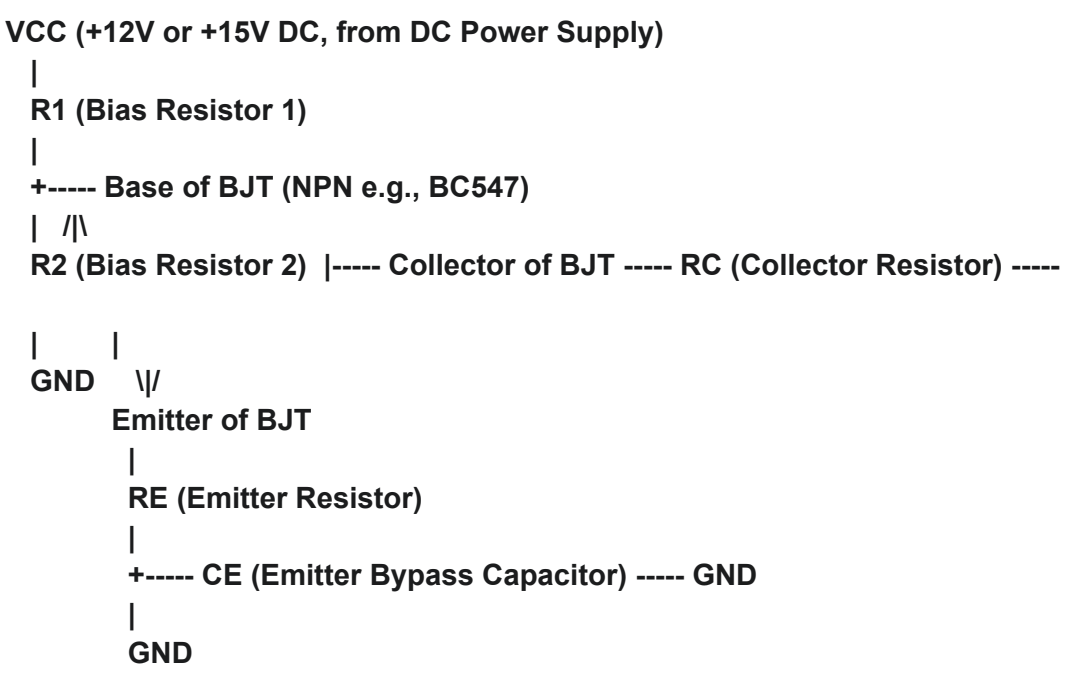
- **Mid-Band Frequency Range: In this region, all coupling capacitors (C_C1, C_C2) and the bypass capacitor (C_E) behave as ideal short circuits (their reactance is negligible). Conversely, the internal parasitic capacitances of the BJT (C_BE, C_BC) behave as open circuits (their reactance is very high). The amplifier achieves its maximum and relatively flat gain.**
- **Low-Frequency Response Roll-off: The gain drops at low frequencies primarily due to the coupling capacitors (C_C1, C_C2) and the bypass capacitor (C_E). At low frequencies, the reactance of these capacitors (X_C=1/(2pifC)) increases significantly, preventing the full AC signal from reaching the amplifier or bypassing the emitter resistor effectively.**

    - **Cutoff Frequencies due to Capacitors: Each capacitor contributes to a lower cutoff frequency. The highest of these frequencies determines the overall lower cutoff frequency (f_L) of the amplifier.**
        - **Input Coupling Capacitor (C_C1): f_L(C1)=frac12piR_in(stage)C_C1, where R_in(stage) is the input resistance of the amplifier stage looking into the base.**
        - **Output Coupling Capacitor (C_C2): f_L(C2)=frac12pi(R_C+R_L)C_C2, where R_L is the external load resistance.**
        - **Emitter Bypass Capacitor (C_E): f_L(CE)=frac12piR_th(C_E)C_E, where R_th(C_E) is the Thevenin resistance seen by C_E (approximately R_E∣∣(r_e′+R_Sig/beta_ac) where R_Sig is the source resistance). This is often the dominant factor for f_L.**
- **High-Frequency Response Roll-off: The gain drops at high frequencies due to the internal parasitic capacitances of the BJT (e.g., C_BE and C_BC or C_pi and C_mu in the hybrid-pi model) and any stray wiring capacitances. At high frequencies, the reactance of these small capacitances decreases, effectively "shorting out" or shunting the signal path, leading to a reduction in gain.**
    - **Miller Effect: The capacitor C_BC (or C_mu) between the base and collector is particularly problematic. Due to the amplifier's gain, this capacitance appears much larger when viewed from the input, an effect known as the Miller effect. This significantly reduces the effective input impedance and thus the gain at high frequencies.**
    - **The lowest of the high-frequency cutoff frequencies due to various parasitic capacitances determines the overall upper cutoff frequency (f_H). The calculations are complex and often involve the hybrid-pi model.**
- **Gain in Decibels (dB): For plotting frequency response, gain is conveniently expressed in decibels (dB) due to the wide range of gain values. Voltage Gain in dB (A_v(dB)) = 20log_10(∣A_v∣)**
- **Cutoff Frequencies (f_L and f_H) and Bandwidth (BW):**
    - **Cutoff Frequencies (Half-Power Frequencies / -3 dB Frequencies): These are the frequencies at which the amplifier's gain drops to 0.707 times (or 1/sqrt2) of its maximum mid-band gain. In decibels, this corresponds to a 3 dB drop from the mid-band gain.**
        - **A_v(f_L)=A_v(mid−band)−3textdB**
        - **A_v(f_H)=A_v(mid−band)−3textdB**
    - **Bandwidth (BW): The range of frequencies over which the amplifier's gain is at least 3 dB below its mid-band maximum. BW=f_H−f_L A wider bandwidth indicates that the amplifier can amplify a broader range of signal frequencies effectively without significant attenuation.**

5.0 CIRCUIT DIAGRAM:

Figure 3.1: Common-Emitter BJT Amplifier with Voltage Divider Bias

This schematic illustrates the complete CE amplifier circuit, including DC biasing components, AC coupling, and bypass capacitors.



Input Side Circuitry:
AC Function Generator --> Cc1 (Input Coupling Capacitor) --> Base of BJT
(Connect Oscilloscope Channel 1 probe here, i.e., at Base of BJT, after Cc1)

Output Side Circuitry:
Collector of BJT --- Cc2 (Output Coupling Capacitor) --> RL (Load Resistor) --> GND
V_out (Measure across RL with Oscilloscope Channel 2)

Note: The component labels (R1, R2, RC, RE, Cc1, Cc2, Ce) correspond to the theoretical design.

6.0 PROCEDURE:

Follow these systematic steps to design, build, and characterize your BJT amplifier. Ensure proper safety measures, especially when dealing with power supplies.

Part A: DC Biasing Design and Q-point Measurement

1. **Theoretical Design of DC Biasing Circuit:**
    - **Specify Design Goals: For an NPN BC547 transistor, aim for a stable DC operating point (Q-point) with approximate values:**
        - **I_Capprox2textmA**
        - **V_CEapproxV_CC/2 (assuming V_CC=12V, so V_CEapprox6V)**

- **Assume BJT Parameters: Take a typical beta_DC for BC547 (e.g., beta_DC=150). Assume V_BE=0.7V.**
- **Calculate Resistor Values: Follow the detailed steps outlined in Section 4.2.1 ("DC Analysis Steps") to determine appropriate standard resistor values for R_1, R_2, R_C, and R_E.**
- **Select Capacitors: Choose suitable electrolytic capacitors for coupling (C_C1, C_C2, typically 1 µF or 10 µF) and bypass (C_E, typically 100 µF or 470 µF). Ensure their voltage ratings are sufficient (e.g., 25V or 50V for a 12V V_CC).**
- **Record your calculated and chosen component values in Observation Table 7.1.**

2. **Circuit Construction (DC Bias Only):**
   - **Carefully assemble the DC biasing part of the common-emitter amplifier on the breadboard (excluding the AC input/output components initially).**
   - **Double-check all resistor values using a DMM before placing them.**
   - **Ensure the NPN BJT's pinout (Emitter, Base, Collector) is correct and matches the datasheet for your BC547.**
   - **Verify the polarity of any electrolytic capacitors if connected.**
3. **DC Q-point Measurement:**
   - **Connect the DC Power Supply and set it to your designed V_CC (e.g., +12V).**
   - **Measure DC Voltages: Using a DMM in DC voltage mode, measure the quiescent (no-signal) DC voltages at:**
     - **Base (V_B)**
     - **Emitter (V_E)**
     - **Collector (V_C)**
     - **Collector-Emitter (V_CE=V_C−V_E)**
   - **Measure DC Current: Measure the quiescent DC collector current (I_C). This can be done by measuring the voltage drop across R_C (V_RC) and then calculating I_C=V_RC/R_C.**
   - **Record all measured DC values in Observation Table 7.2.**
   - **Compare: Compare these measured values with your theoretically calculated design values. Small discrepancies are expected due to component tolerances and variations in the actual beta of the transistor.**

Part B: AC Mid-Band Analysis (Gain and Impedances)

1. **Complete Circuit Assembly:**
   - **With the DC power supply OFF, integrate the AC input coupling capacitor (C_C1), the output coupling capacitor (C_C2), the emitter bypass capacitor (C_E), and the load resistor (R_L, e.g., 10 kΩ or 15 kΩ) into your breadboard circuit as shown in Figure 3.1. Ensure all capacitor polarities are correct.**
   - **A typical R_L for a small signal amplifier is often selected to represent the input impedance of the next stage or a standard oscilloscope probe impedance (e.g. 1M Ohm). For this experiment, using a discrete resistor value like 10kOhm is fine.**
2. **Theoretical Mid-Band Parameter Calculation:**

- **Based on your measured I_E (from Part A.3), calculate the experimental r_e′ using r_e′=V_T/I_E (where V_Tapprox26textmV).**
- **Using this r_e′ and your assumed beta_ac (e.g., 150), calculate the theoretical mid-band voltage gain (A_v), input resistance (R_in), and output resistance (R_out) using the formulas provided in Section 4.3.**
- **Record these theoretical AC values in Observation Table 7.3.**

3. **Mid-Band Voltage Gain (A_v) Measurement:**
   - **Power on the DC supply (V_CC).**
   - **Connect the AC Function Generator to the input of the amplifier (before C_C1, or between C_C1 and the base) and set it to produce a sinusoidal waveform with a small peak-to-peak amplitude (e.g., 20-50 mV p-p).**
   - **Set the frequency to a mid-band value (e.g., 5 kHz or 10 kHz). Choose a frequency where the gain is relatively stable (not affected by coupling/bypass caps or parasitic caps).**
   - **Connect Channel 1 of the Oscilloscope to the actual amplifier input (i.e., at the base of the BJT, *after* C_C1) to measure V_in(p−p).**
   - **Connect Channel 2 of the Oscilloscope to the output of the amplifier (across the load resistor R_L) to measure V_out(p−p).**
   - **Ensure both oscilloscope channels are set to AC coupling for accurate AC signal measurement. Adjust the Volts/Div and Time/Div settings for clear waveform visualization.**
   - **Measure the peak-to-peak input voltage (V_in(p−p)) and the peak-to-peak output voltage (V_out(p−p)).**
   - **Calculate the experimental mid-band voltage gain: A_v=fracV_out(p−p)V_in(p−p).**
   - **Observe and note the phase relationship between the input and output waveforms (a 180-degree phase shift is expected for CE).**
   - **Record the measured A_v in Observation Table 7.3. Convert it to dB: A_v(dB)=20log_10(∣A_v∣).**
4. **Input Resistance (R_in) Measurement (Source Resistance Method):**
   - **Ensure the Function Generator is connected to the amplifier input through C_C1.**
   - **Connect a known variable resistor (or a decade resistance box) R_S in series with the function generator output and the amplifier input (i.e., between the Function Generator and C_C1). Initially set R_S=0Omega.**
   - **Apply a mid-band AC input signal with a convenient amplitude.**
   - **Measure the input voltage at the base of the BJT (V_in) using the oscilloscope when R_S=0. Record this as V_in(0).**
   - **Now, increase the value of R_S until the input voltage at the base (V_in) drops to exactly half of V_in(0). At this point, the value of the series resistor R_S is equal to the input resistance of the amplifier: R_in=R_S.**
   - **Alternatively, measure V_in (at base) with R_S=0 (V_in0) and then with R_S=R_S′ (a known value) (V_in′). Then calculate R_in=R_S′left(fracV_in0V_in′−1right).**
   - **Record the measured R_in in Observation Table 7.3. Compare it to your theoretical calculation.**
5. **Output Resistance (R_out) Measurement (Load Resistance Method):**

- **Remove any external load resistor R_L connected to the amplifier output (if present, measure V_{out} right after C_{C2}). This is your open-circuit output voltage ($V_{out(OC)}$).**
- **Now, connect a known variable load resistor (R_L', e.g., a potentiometer or decade box) at the output (across the output terminals, after C_{C2} and parallel to the internal output resistance).**
- **Apply a mid-band input signal.**
- **Adjust R_L' until the output voltage (V_{out}) drops to half of the previously measured $V_{out(OC)}$. At this point, the value of R_L' is equal to the output resistance of the amplifier: $R_{out}=R_L'$.**
- **Record the measured R_{out} in Observation Table 7.3. Compare it to your theoretical calculation.**

Part C: Frequency Response Plotting and Bandwidth Determination

1. **Setup for Frequency Response:**
   - **Ensure the amplifier circuit is fully assembled as in Figure 3.1.**
   - **Connect Channel 1 of the Oscilloscope to the amplifier input (base), and Channel 2 to the amplifier output (across R_L).**
   - **Set the Function Generator to produce a constant peak-to-peak amplitude (e.g., 20-50 mV p-p) AC input signal. It is crucial that the input amplitude remains constant throughout the frequency sweep.**
   - **Set the oscilloscope channels to AC coupling.**
2. **Data Collection for Frequency Response:**
   - **Start at a very low frequency (e.g., 10 Hz). Measure $V_{in(p-p)}$ and $V_{out(p-p)}$. Calculate the voltage gain ($A_v=V_{out}/V_{in}$) and convert it to dB ($20\log_{10}|A_v|$).**
   - **Gradually increase the input frequency across a wide range (e.g., from 10 Hz to 1 MHz), taking more readings in regions where the gain is changing rapidly (at low and high frequencies) and fewer readings in the mid-band region where the gain is relatively flat.**
   - **For each frequency step, ensure $V_{in(p-p)}$ remains constant. Read $V_{out(p-p)}$ and calculate the gain in dB.**
   - **Record all frequency points, input/output voltages, and calculated gains in Observation Table 7.4.**
3. **Frequency Response Plotting (Bode Plot):**
   - **Using the data from Observation Table 7.4, plot the Gain in dB (on the Y-axis) against Frequency (on the X-axis) on a semi-log graph paper. The frequency axis MUST be logarithmic.**
   - **Clearly label the axes and indicate the units.**
4. **Bandwidth Determination from Plot:**
   - **Identify the maximum gain in dB from your plot. This is your Mid-Band Gain ($A_{v(mid-band)}$ in dB).**
   - **Calculate the -3 dB gain level: $A_{v(-3dB)}=A_{v(mid-band)}-3\text{dB}$.**
   - **Draw a horizontal line on your graph at this -3 dB gain level.**
   - **Locate the two frequencies where your gain curve intersects this -3 dB line. These are your Lower Cutoff Frequency (f_L) and Upper Cutoff Frequency (f_H).**

- **Calculate the Bandwidth (BW): $BW = f_H - f_L$.**
- **Record f_L, f_H, and BW in Observation Table 7.4.**

Part D: Effect of Capacitors (Qualitative Observation and Discussion)

1. **Effect of Removing Bypass Capacitor (C_E):**
   - **With the DC power supply OFF, temporarily remove the emitter bypass capacitor (C_E) from the circuit.**
   - **Power on the DC supply. Apply a mid-band AC input signal (same as used for mid-band gain measurement in Part B).**
   - **Observe the output voltage (V_{out}) on the oscilloscope.**
   - **Qualitatively describe the change in amplifier gain. Explain why removing C_E affects the gain.**
2. **Effect of Changing Coupling Capacitors (C_{C1}, C_{C2}):**
   - **Power off the DC supply. Reconnect C_E.**
   - **Replace either C_{C1} or C_{C2} with a significantly smaller value (e.g., if you used 10 µF, replace it with 1 µF or even 0.1 µF, ensuring correct polarity).**
   - **Power on the DC supply. Apply an AC input signal.**
   - **Focus on the low-frequency region of the frequency response. Observe how the output voltage behaves at low frequencies compared to your original setup. You can quickly sweep frequencies downwards from mid-band to see the roll-off.**
   - **Qualitatively describe how changing the coupling capacitor value affects the lower cutoff frequency (f_L). Explain why this happens.**

7.0 OBSERVATIONS AND READINGS:

7.1 Component Values Used:

Record the specific resistor and capacitor values you selected and used in your circuit. Measure them with a DMM if possible to get actual values.

Component	Value (Designed/Calculated)	Value (Measured/Used in Circuit)
V_{CC} (Supply)	12 V	_____ V
R_1	_____ Ω	_____ Ω
R_2	_____ Ω	_____ Ω
R_C	_____ Ω	_____ Ω
R_E	_____ Ω	_____ Ω
C_{C1} (Input Coupling)	_____ µF	_____ µF

C_C2 (Output Coupling)	_____ µF	_____ µF
C_E (Emitter Bypass)	_____ µF	_____ µF
R_L (Load Resistor)	_____ Ω	_____ Ω
BJT Type	BC547 NPN	BC547 NPN

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7.2 DC Biasing (Q-point) Measurements:

Record your calculated DC bias values and compare them with your actual measurements.

Parameter	Calculated Value (from Design)	Measured Value (from Circuit)	Remarks/Comparison
V_B (Base Voltage)	_____ V	_____ V	
V_E (Emitter Voltage)	_____ V	_____ V	
V_C (Collector Voltage)	_____ V	_____ V	
V_CE (Collector-Emitter Voltage)	_____ V	_____ V	
I_C (Collector Current)	_____ mA	_____ mA	

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7.3 AC Mid-Band Performance Measurements:

Record your theoretical calculations and experimental measurements for AC gain and impedances.

- Mid-Band Frequency (f_mid used for reference): _____ kHz
- Calculated r_e′ (using measured I_E): _____ Ω
- Assumed beta for calculations: _____

Parameter	Calculated Theoretical Value	Measured Experimental Value	Remarks/Comparison
V_in(p−p) (Input at Base, Oscilloscope)	N/A	_____ V	

V_out(p−p) (Output across R_L, Oscilloscope)	**N/A**	**_____ V**	
Mid-Band Voltage Gain (A_v) (V_out/V_in)	**_____**	**_____**	
Mid-Band Voltage Gain (A_v in dB)	**_____ dB**	**_____ dB**	
Input Resistance (R_in)	**_____ Ω**	**_____ Ω**	
Output Resistance (R_out)	**_____ Ω**	**_____ Ω**	
Phase Shift (Input to Output)	**180 Degrees**	**_____ Degrees**	**(Observe on Scope)**

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7.4 Frequency Response Data:

Record the frequency sweep data used to plot the Bode plot.

- **Mid-Band Gain (A_v(mid−band)): _____ (V/V ratio)**
- **Mid-Band Gain (A_v(mid−band) in dB): _____ dB (Used as reference for -3dB points)**

| S. No. | Frequency (f) (Hz/kHz) | V_in(p−p) (V) | V_out(p−p) (V) | Voltage Gain (A_v) (V_out(p−p)/V_in(p−p)) | Gain in dB (20log_10(∣A_v∣)) | Remarks (e.g., "Low Freq", "Mid-band", "High Freq") | | :----- | :---------- | :---------- | :---------- | :---------- | :---------- | | I. Low Frequency Region (Gain Rolling Off) | | 1 | | | | | | | 2 | | | | | | | ... | (Approx. 5-10 data points or more depending on roll-off steepness) | | II. Mid-Band Frequency Region (Gain Flat/Constant) | | 1 | | | | | | | 2 | | | | | | | ... | (Approx. 5-10 data points) | | III. High Frequency Region (Gain Rolling Off) | | 1 | | | | | | | 2 | | | | | | | ... | (Approx. 5-10 data points or more depending on roll-off steepness) |

- **From Frequency Response Plot (After plotting Graph 3.1):**
  - **Lower Cutoff Frequency (f_L): _____ Hz (Frequency where gain drops by 3 dB from mid-band gain)**
  - **Upper Cutoff Frequency (f_H): _____ Hz (Frequency where gain drops by 3 dB from mid-band gain)**
  - **Bandwidth (BW=f_H−f_L): _____ Hz**

7.5 Qualitative Observations (Effect of Capacitors):

Record your observations and initial thoughts on the capacitor effects.

- **Observation 1 (Effect of Removing Emitter Bypass Capacitor C_E):**

    - **Describe the change in output voltage (and thus gain) observed at mid-band frequency when C_E was removed:**

- **Observation 2 (Effect of Changing Coupling Capacitors C_C1/ C_C2 to a Smaller Value):**
    - **Describe the change in the low-frequency response observed (e.g., how did f_L shift, or how did gain behave at lower frequencies):**

8.0 GRAPHS:

Include the following graph(s) based on your experimental data. Use appropriate labels and scales.

- **Graph 3.1: Frequency Response (Bode Plot)**
    - **Type: Semi-log graph (logarithmic X-axis for frequency, linear Y-axis for gain in dB).**
    - **Data Source: Use the data from Observation Table 7.4.**
    - **Plot: Plot Gain in dB (Y-axis) versus Frequency (X-axis).**
    - **Markings: Clearly mark the Mid-Band Gain, the -3 dB gain level, and identify the Lower Cutoff Frequency (f_L) and Upper Cutoff Frequency (f_H) on the graph. Draw lines to show how f_L and f_H are determined from the -3 dB points.**

9.0 CALCULATIONS:

Provide detailed steps for all calculations performed in this experiment.

9.1 DC Biasing Calculations (Based on Design Values from 7.1):

- **Target I_C: [Value] mA**
- **Target V_CE: [Value] V**
- **Assumed beta_DC: [Value]**
- **Step-by-step calculation of R_1,R_2,R_C,R_E as performed in Part A.1 of Procedure.**
    - **(Show calculations for V_E, I_E, V_B, R_E, R_2, R_1, R_C)**

9.2 AC Small-Signal Parameter Calculations (Mid-Band, Based on Measured DC Q-point from 7.2):

- **Measured I_E (from 7.2): [Value] mA**
- **Thermal Voltage (V_T): Approximately 26 mV at room temperature.**
- **Calculation of AC Emitter Resistance (r_e′): r_e′=V_T/I_E = [Your Calculation] Ω**
- **Assumed beta_ac (for AC analysis, typically approxbeta_DC): [Value]**
- **Calculation of Theoretical Mid-Band Voltage Gain (A_v): A_v=−fracR_C∣∣R_Lr_e′ (Where R_C and R_L are from 7.1, R_L is the external load) $A_v = $ [Your Calculation] (ratio) A_v(dB)=20log_10(∣A_v∣) = [Your Calculation] dB**
- **Calculation of Theoretical Input Resistance (R_in): R_B=R_1∣∣R_2=fracR_1timesR_2R_1+R_2 (using values from 7.1) $R_B = $ [Your Calculation] Ω R_in=R_B∣∣(beta_acr_e′)=fracR_Btimes(beta_acr_e′)R_B+(beta_acr_e′) $R_{in} = $ [Your Calculation] Ω**
- **Calculation of Theoretical Output Resistance (R_out): R_out=R_C (using value from 7.1) $R_{out} = $ [Your Calculation] Ω**

9.3 Bandwidth Calculations (Based on Frequency Response Plot Data from 7.4):

- **Mid-Band Gain (A_v(mid−band) in dB): [Value from graph] dB**
- **-3 dB Gain Level: A_v(−3dB)=A_v(mid−band)−3textdB = [Your Calculation] dB**
- **Lower Cutoff Frequency (f_L): [Value from graph] Hz**
- **Upper Cutoff Frequency (f_H): [Value from graph] Hz**
- **Bandwidth (BW): BW=f_H−f_L = [Your Calculation] Hz**

10.0 RESULTS:

Present the significant numerical results obtained from the experiment in a clear and concise manner.

- **DC Operating Point (Q-point):**
  - **Measured Collector Current (I_C): [Your Value] mA**
  - **Measured Collector-Emitter Voltage (V_CE): [Your Value] V**
- **AC Mid-Band Performance:**
  - **Measured Mid-Band Voltage Gain (A_v): [Your Value] (or [Your Value] dB)**
  - **Measured Input Resistance (R_in): [Your Value] Ω**
  - **Measured Output Resistance (R_out): [Your Value] Ω**
- **Frequency Response Characteristics:**
  - **Lower Cutoff Frequency (f_L): [Your Value] Hz**
  - **Upper Cutoff Frequency (f_H): [Your Value] Hz**
  - **Bandwidth (BW): [Your Value] Hz**

11.0 DISCUSSION AND ANALYSIS:

This is the most critical section where you interpret your results, compare them with theoretical expectations, explain observed phenomena, and discuss any discrepancies.

1. **DC Biasing Evaluation:**
    - **Comparison: Compare your experimentally measured Q-point (I_C, V_CE) with your theoretically designed Q-point values. Discuss the percentage difference for each parameter.**
    - **Discrepancies: Identify and explain potential reasons for any discrepancies between measured and calculated DC values (e.g., component tolerances, actual beta_DC of the specific BJT which might differ from assumed value, loading effects of the DMM).**
    - **Bias Stability: Explain why the voltage divider bias method is considered robust and stable for establishing the Q-point compared to simpler biasing schemes.**
2. **Mid-Band Amplifier Performance Analysis:**
    - **Voltage Gain: Compare your experimentally measured mid-band voltage gain (A_v) with its theoretically calculated value. Discuss the accuracy of the r-e model for predicting gain in this range. Did you observe the expected 180-degree phase shift? Explain the physical reason for this phase inversion in a common-emitter configuration.**
    - **Input and Output Impedances: Compare your experimentally measured input resistance (R_in) and output resistance (R_out) with their theoretical values. Discuss any differences. Explain the practical significance of R_in (e.g., loading effect on the signal source) and R_out (e.g., driving capability for the load).**
3. **Frequency Response Characteristics:**
    - **Bode Plot Interpretation: Describe the overall shape of your frequency response curve (Bode plot). Clearly delineate the low-frequency, mid-band, and high-frequency regions.**
    - **Low-Frequency Roll-off Explanation:**
        - **Identify the specific capacitors responsible for the gain roll-off at low frequencies (C_C1,C_C2,C_E). Explain the mechanism: how does the increasing reactance of these capacitors at lower frequencies lead to reduced gain?**
        - **Effect of Bypass Capacitor (C_E): Based on your observation in Part D.1, explain in detail why removing C_E drastically reduces the mid-band voltage gain. What is the fundamental purpose of C_E?**
        - **Effect of Coupling Capacitors (C_C1,C_C2): Based on your observation in Part D.2, explain how the value of coupling capacitors influences the lower cutoff frequency (f_L). Why does a smaller capacitance lead to a higher f_L?**
    - **High-Frequency Roll-off Explanation:**
        - **Identify the primary reasons for the gain roll-off at high frequencies (i.e., internal parasitic capacitances of the BJT, C_BE and C_BC).**

        - **Explain the qualitative effect of these capacitances: how do they effectively "short-circuit" the signal path at high frequencies, leading to reduced gain?**
        - **Briefly mention the concept of the Miller effect and its impact on the input capacitance at high frequencies.**
    - **Bandwidth Analysis:**
        - **Discuss the significance of the amplifier's bandwidth (BW). What does a wider bandwidth imply in terms of the amplifier's ability to process signals?**
        - **Relate your determined f_L and f_H to the overall bandwidth.**
4. **Sources of Error and Limitations:**
    - **Identify potential sources of experimental error that might have affected your results (e.g., tolerance of resistors and capacitors, imprecise measurement techniques, internal resistance of signal generator/oscilloscope, loading effects of probes, breadboard parasitic capacitances, ambient temperature variations affecting BJT parameters).**
    - **Discuss how these errors could lead to deviations between theoretical calculations and experimental measurements.**
    - **Comment on the limitations of the simple r-e model used for theoretical analysis, especially at very high frequencies.**

12.0 CONCLUSION:

Conclude your experiment by summarizing the key learning outcomes and reinforcing the understanding gained.

This experiment successfully demonstrated the comprehensive design, construction, and characterization of a single-stage common-emitter BJT amplifier. Through systematic DC biasing, we achieved a stable operating point crucial for linear amplification. The mid-band voltage gain, input resistance, and output resistance were accurately measured and found to be in reasonable agreement with theoretical predictions based on the r-e model. Crucially, the frequency response analysis, visualized through the Bode plot, clearly illustrated the amplifier's gain roll-off at both low and high frequencies. We successfully identified the lower (f_L) and upper (f_H) cutoff frequencies and determined the amplifier's bandwidth. Furthermore, the practical observations highlighted the critical role of coupling and bypass capacitors in defining the amplifier's frequency characteristics. This experiment has provided invaluable practical insight into BJT amplifier operation, its frequency limitations, and the fundamental principles of analog circuit design.